Amendment of Claims:

This listing of claims will replace all prior versions and listings, of claims in the application.

1. (Previously presented) An apparatus comprising:

a control word predictor to predict a predicted control word for execution of a plurality of operations in response to a control word changing operation;

execution resources to speculatively execute the plurality of operations utilizing the predicted control word;

a comparison module to determine if an actual control word matches the predicted control word set by the control word changing operation or a plurality of other control words stored in a storage element, and to cause re-execution of said plurality of operations if said actual control word matches any of the plurality of other control words.

2. (Original) The apparatus of claim 1 wherein a match by said comparison module to any of the plurality of other control words causes re-execution of said plurality of operations substantially according to a branch misprediction process.

3. (Original) The apparatus of claim 2 wherein a mismatch of the actual control

word to all the plurality of other control words and the predicted control word causes a serialization process substantially more time consuming than said branch misprediction process.

4. (Original) The apparatus of claim 3 wherein said control word predictor comprises a prediction table.

5. (Original) The apparatus of claim 1 further comprising:
means for adjusting the control word predictor to predict the actual control word during re-execution of said plurality of operations.

6. (Original) The apparatus of claim 1 wherein said control word predictor comprises a prediction table, wherein said apparatus further comprises a microsequencer to dispatch a set operation to change an entry in said prediction table if said actual control word matches any of the plurality of other control words.

7. (Original) The apparatus of claim 1 further comprising:
a microsequencer to generate one or more first operations in response to said control word changing operation, the one or more first operations to provide a conditional branch based on whether or not the predicted control word matches the actual control word, and wherein said microsequencer is to generate a second operation if the predicted control

word does not match the actual control word but matches one of the plurality of other control words, said second operation to alter a prediction of the control word predictor.

8. (Original) The apparatus of claim 6 wherein said actual control word is a floating point control word, and wherein said one or more first operations and said second operation are microoperations, and further wherein said control word changing operation is a load floating point control word macroinstruction.

9. (Original) The apparatus of claim 1 wherein processor comprises data embodied on a machine readable medium.

10. (Previously presented) A method comprising:

generating a predicted control word in response to a control word changing operation;

executing a plurality of operations using the predicted control word;

testing whether an actual control word matches said predicted control word or one of a plurality of other control words stored in a storage element;

updating a prediction if the actual control word matches one of the plurality of other control words; and

re-executing said plurality of operations if the predicted control word matches one of the plurality of other control words.

11. (Canceled)

12. (Original) The method of claim 10 further comprising:

treating said plurality of operations as a plurality of dependent instructions on a mispredicted branch if the predicted control word matches one of the plurality of other control words.

13. (Original) The method of claim 10 further comprising:

selecting the predicted control word from a prediction table from a table location based on an instruction pointer to generate the predicted control word;

speculatively executing a plurality of operations with said predicted control word after selecting the predicted control word from the prediction table.

14. (Original) The method of claim 13 wherein selecting comprises tagging a microoperation with a table entry number indicative of which control word is selected from the prediction table.

15. (Original) The method of claim 14 wherein updating the prediction comprises:

generating a set microoperation to set the table location to indicate the actual control word.

16. (Original) The method of claim 15 further comprising:

performing a serializing flow if the actual control word mismatches both the plurality of other control words and the predicted control word.

17. (Original) The method of claim 10 wherein said control word changing operation comprises a load floating point control word instruction, the method further comprising:

decoding the load floating point control word instruction to generate a test microoperation and optionally a set operation to update the prediction if the actual control word matches one of the plurality of other control words

18. (Previously presented) A system comprising:

a memory to store a control word changing instruction and a plurality of programmatically subsequent instructions;

a processor including control word prediction logic, said processor to predict a predicted control word in response to said control word changing instruction and to speculatively execute said plurality of programmatically subsequent instructions, said processor using a first recovery mechanism if a later determined actual control word mismatches the predicted control word but matches one of a plurality of stored control words stored in a storage element, and using a second recovery mechanism if said later determined actual control word mismatches the predicted control word and the plurality of stored control words.

19. (Original) The system of claim 18 further comprising:

a communications interface.

20. (Original) The system of claim 19 wherein said control word changing instruction is downloaded via the communications interface prior to execution by the processor.

21. (Original) The system of claim 20 wherein the first recovery mechanism utilizes a branch misprediction recovery technique and said second recovery mechanism utilizes a serialization technique.

22. (Original) The system of claim 18 wherein first recovery mechanism utilizes a branch misprediction recovery technique and said second recovery mechanism utilizes a serialization technique.

23. (Previously presented) A processor comprising:

a front end instruction decoder to decode a control word changing instruction;

control word prediction logic to provide a predicted control word in response to said control word changing instruction;

allocation logic to allocate register resources and to generate colors for instructions, said allocation logic to cause a color change for a plurality of instructions subsequent to said control word changing instruction;

scheduling logic to schedule execution of said plurality of instructions

subsequent to said control word changing instruction;

execution logic coupled to said scheduling logic to speculatively execute said plurality of instructions subsequent to said control word changing instruction using said predicted control word;

comparison logic to compare an actual control word to said predicted control word and to a plurality of control words, if said actual control word matches one of the plurality of control words, said comparison logic to signal said control word prediction logic and to trigger re-execution of said plurality of instructions subsequent to said control word changing instruction using said predicted control word.

24. (Original) The processor of claim 23 further comprising a microinstruction sequencer, wherein said microinstruction sequencer generates:

a test microinstruction to test whether the actual control word matches the predicted control word;

a set microinstruction to update a prediction in the control word prediction logic if said actual control word matches one of the plurality of control words.

25. (Original) The processor of claim 24 wherein said microinstruction sequencer further generates, if the actual control word mismatches the plurality of control words:

a serializing microinstruction flow if said actual control word mismatches

all of said plurality of control words.

26. (Previously presented) The apparatus of claim 1, wherein the plurality of other control words are stored in a storage element.

27. (Previously presented) The system of claim 18, wherein the plurality of other control words are stored in a control word storage.